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# Field-store standards conversion:
## Servo-control of the field delay

No. 1970/16

Research Department, Engineering Division
THE BRITISH BROADCASTING CORPORATION

RESEARCH DEPARTMENT

# FIELD-STORE STANDARDS CONVERSION: SERVO-CONTROL OF THE FIELD DELAY

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# FIELD-STORE STANDARDS CONVERSION: SERVO-CONTROL OF THE FIELD DELAY

## SUMMARY

*A servo-control system is described which maintains the duration of a field delay equal to the field duration of the applied television signal. Errors in delay are corrected by binary-related lengths of coaxial cable which are switched into or out of circuit, as required. Since the range of control is insufficient using practical lengths of cable, several quartz delays are also included to accommodate larger errors. Delay errors are detected by comparing the timing of line synchronising pulses at the input and output of the delay and adjustments are made in steps of 9 ns.*

## 1. INTRODUCTION

Delays having a duration of one television line have found applications in television signal processing, e.g. vertical aperture correction[1] and line store standards conversion.[2] A number of applications have also been suggested for delays having a duration of one television field, notably in improved vertical aperture correction, film telerecording and standards conversion.

The construction of a field delay is considerably more difficult and costly than the construction of a line delay and a field delay of satisfactory quality for television signal transmission has only recently been produced.[3] Such a field delay is used in the advanced field-store standards converters[4,5] as a means of obtaining simultaneously, signals from two successive fields for the purposes of interpolation.[6]

In general the uses of field delays require that the delayed and undelayed signals should be so aligned that the picture elements corresponding to a particular vertical narrow strip of the picture shall coincide in time. A timing accuracy of approximately 10 ns is required for monochrome signals and a similar accuracy is required to mix composite colour signals. To satisfy this requirement it is necessary to control the duration of the delay so that it shall be equal to the field duration* over the range of field frequencies encountered in practice.

For monochrome signals which may be locked in frequency to the mains supply, variations in field duration of many microseconds are encountered. Colour signals are almost invariably crystal controlled and the variation of field duration seldom exceeds a few hundred nanoseconds.

This report describes a servo-controlled system which enables the duration of a field delay to be varied in synchronism with the field duration.

## 2. PRINCIPLES OF THE DELAY CONTROL SYSTEM

The system operates by detecting the presence of an error in the delay and correcting it by switching delay in or out of circuit as required.

The error-detection system compares the timing of line synchronising pulses at the input and output of the field delay. Three conditions are possible. Firstly, the line synchronising pulses at the input to the field delay may be ahead of those at the output in which case the delay is too long. Secondly, the line synchronising pulses at the input may be behind those at the output in which case the delay is too short. Thirdly, the line synchronising pulses may be so close to each other in time that the delay is within the specified tolerance of its desired duration. A signal having three distinguishable states is therefore produced by an error-detection system, each time the synchronising pulses are compared. According to the state of this signal, delay is added or subtracted from the delay, as necessary, by switching into and out of circuit discrete units of delay. Thus, for example, at the time of a synchronising pulse comparison, if the delay is found to be too short, one unit is switched into circuit. At the time of the next comparison, the delay may now be within tolerance in which case no further changes are made, or it may still be too short in which case a further unit of delay must be added. A similar action takes place if the delay is too long except that in this case the delay is reduced in discrete steps instead of being increased.

It is clearly essential that the unit of switched delay is smaller than the tolerance, otherwise the delay duration will continually hunt between two values, both of which may be outside the tolerance.

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* The actual delay required may be one field plus or minus a half-line because of interlace.

The main practical problem encountered is the production of a switchable delay store of sufficient capacity to accommodate the maximum total change required. For colour signals, with tightly controlled scanning frequencies, the variations are not more than a few hundred nanoseconds and can adequately be compensated using the delay obtained from a few hundred feet of co-axial cable. For monochrome signals, however, variations of several microseconds might be required and the length of coaxial cable needed would be prohibitive.

To accommodate such larger changes, larger delay elements can be switched into the signal path in addition to the switchable cable delays. These consist of quartz delays whose durations are in arithmetic progression, the difference being somewhat less than the capacity of the switchable cable delays. One of these quartz delays is always in circuit and if the total delay is required to increase beyond the range of the switchable cable delay, a longer quartz delay is switched into circuit and the cables switched almost to their minimum value allowing a further increase through the complete range of the cable delay. Likewise, if the delay is required to be reduced, a shorter quartz delay is switched into circuit.

The choice of line synchronising pulses to carry the timing information results in a possible rate of change of delay of one unit per television line, but has the disadvantage that errors of greater than plus or minus a half-line duration cannot be accommodated since it would be impossible to distinguish between successive line sync. pulses and the control system can lock the total delay to values having errors of an integral number of line-periods. A further refinement could be added in which the field synchronising pulses were also used, to ensure that the correct line synchronising pulse was chosen. However, this refinement has not yet been incorporated nor has it proved necessary.

## 3. PRACTICAL DETAILS OF THE SYSTEM

Fig. 1 shows a block schematic of the system. The video signal is modulated on to an r.f. carrier for transmission through the delay path. The direct signal and the delayed signal are then available for processing at the output terminals. These signals are also fed to two identical demodulators and synchronising pulse separators and the derived synchronising pulses are fed to a timing-comparator. An error signal is generated at the timing comparator and fed to the delay control unit which generates switching signals for the switched cable delays and the switched quartz delays. Switching of the delays occurs during line-synchronising pulses in order to minimise disturbances to the picture.

The action of each of the units of Fig. 1 is described in more detail below.

### 3.1. R.F. Modulation System*

In addition to carrying picture signal information the modulation system has to carry synchronising information to operate the control system. Since the signal may be switched between a number of different paths in the switched delay unit, the use of a.m. would result in the effects of switching being visible on the

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* The use of a r.f. modulator system is necessitated by the field delay which has a band-pass response centred on 30 MHz.

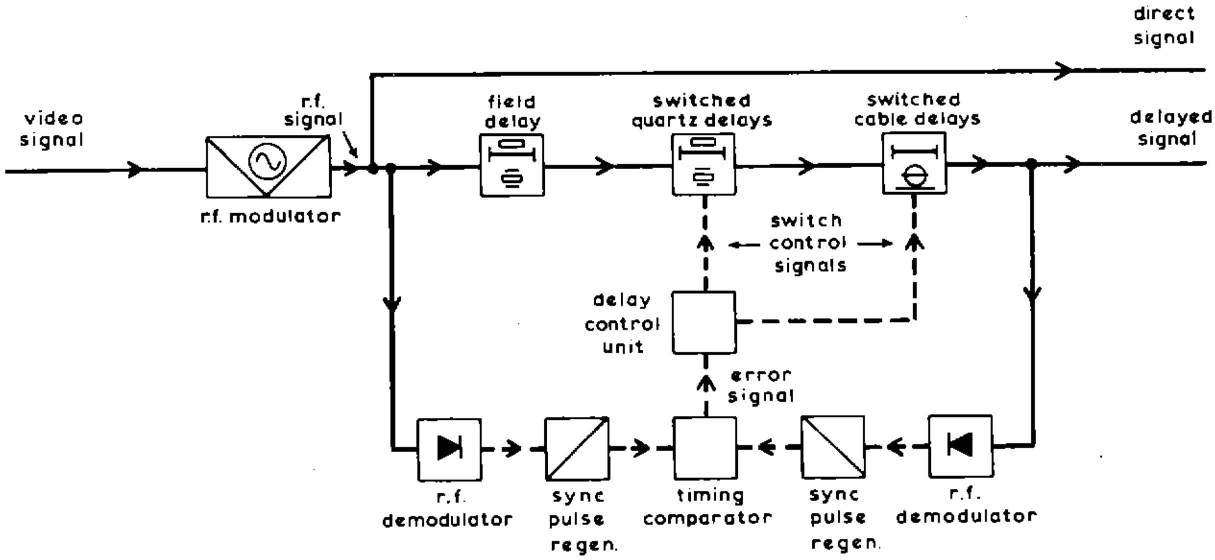

Fig. 1 - Diagram of field delay and servo system

output picture, if the different signal paths had slight gain differences.[9] It was therefore decided to use frequency modulation for the picture signal. If, however, frequency modulation is also used for the sync. pulse information, large changes of phase are liable to occur when the switching takes place and large spurious signals could appear on the demodulated video signal. This would interfere with the process of synchronising pulse separation. Consequently it was decided to use 100% amplitude modulation for transmission of the synchronising pulses.

### 3.2. Field Delay

The field delay consists of several ultrasonic quartz delays[3] in cascade. For the British standard 6 x 3316 μs delays are used making a total of 19·896 ms. For the American standard, 5 x 3316 μs delays are used making a total of 16·580 ms. These values are short of the colour standard field durations by approximately 100 μs each.

### 3.3. Switched Quartz Delays

Fig. 2 shows a diagram of the switched quartz delay system. Four delays of durations 46 μs, 48 μs, 50 μs and 52 μs* are switched in such a way that one is in circuit at any one time. Switching takes place only during the field blanking interval in order to avoid disturbances to the picture.

### 3.4. Switched Cable Delays

Fig. 3 shows a diagram of the switched cable delay system. Eight lengths of coaxial cable are used, their delay durations are in binary relationship to each other starting at 9 ns. The switches S2 to S8 are remotely controlled electronic reversing switches, which connect each input to one of the outputs. By applying the appropriate control voltages to each of the switches it is possible to obtain 256 separate values of delay from 0 to 2·297 μs, in steps of 9 ns.

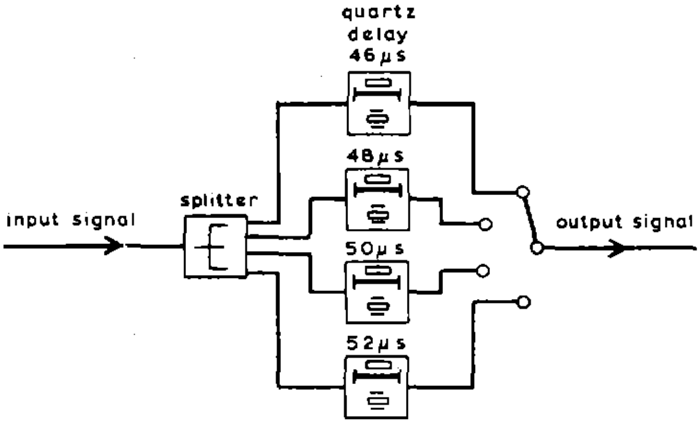

*Fig. 2 - Switched quartz delay system*

### 3.5. Timing Comparison System

As was explained in Section 3.1, 100% a.m. modulation by the line sync. pulses is used to carry timing information. The r.f. demodulators are conventional envelope detectors whose outputs consist of the line synchronising pulses containing the timing information relevant to the input and output signals of the field delay.

Synchronising pulse regenerators are required to abstract the timing information from the demodulated synchronising pulses. The modulated synchronising pulses have a risetime of approximately 200 ns, and being transmitted via an a.m. carrier, are subject to variations of gain in the r.f. transmission paths. The synchronising pulse regenerators determine the time of occurrence of the point of inflexion of the synchronising pulse edge and produce at that time a signal having a timing edge with a rise-time of approximately 10 ns. The timing of the point of inflexion is chosen for this purpose since it is independent of the system gain.

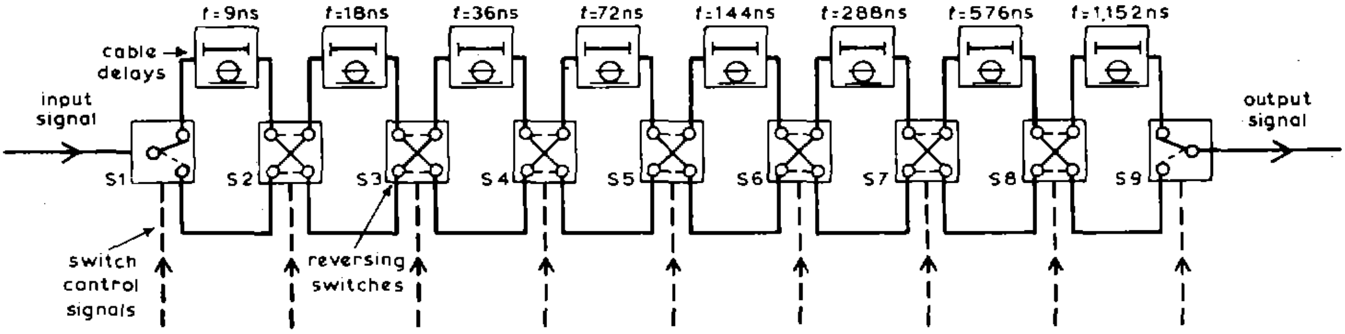

*Fig. 3 - Switched cable delay system*

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* The actual values quoted were chosen to suit the field-store conversion application. In general, as was seen earlier, it is necessary that they are in arithmetic progression.

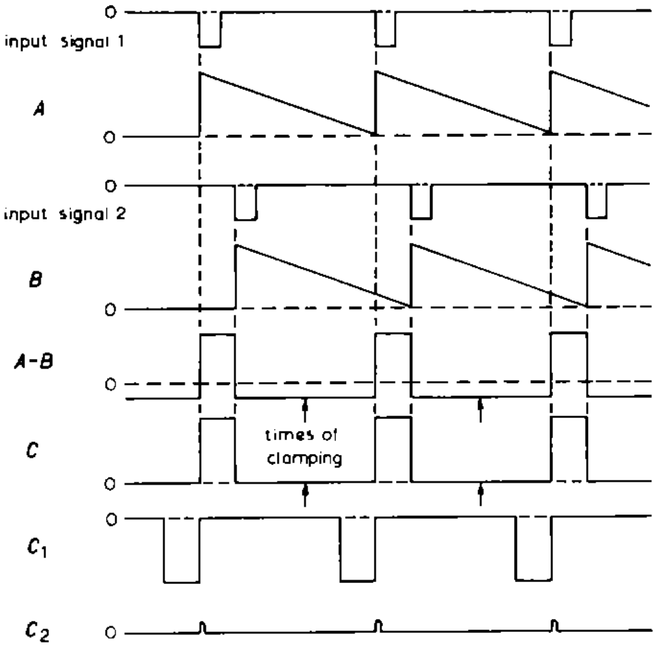

*Fig. 4 - Waveforms associated with timing comparator*

The action of the comparator is described with reference to Fig. 4 which shows waveform diagrams corresponding to signals in the comparator. Each of the input (regenerated) synchronising pulse signals is used to trigger a sawtooth generator. The difference between the resulting sawtooth waveforms, $A$ and $B$, is obtained by subtraction and is then clamped to earth potential at a point in time midway between successive line synchronising pulses obtained from one of the two inputs. The resulting pulse waveform constitutes an error signal and may have various forms, according to the relative timing of the input synchronising pulses.

Waveform $C$ shows the resultant error signal if input signal (2) occurs shortly after input signal (1). Waveform $C_1$ shows the reverse situation. Waveform $C_2$ shows the error signal when the timings of the two input signals are very close – closer, in fact, than the duration of the retrace times of the sawtooth waveforms, $A$. and $B$. The three possible states like $C$, $C_1$ and $C_2$ are distinguished by means of level discriminators whose outputs trigger two bistable circuits when the error pulses are greater than a controlled magnitude; in the positive direction in one case to describe an error in one direction, and in the negative direction in the other case to describe an error in the other direction. Thus the three possible states are described by the states of two bistable devices.

### 3.6. Delay Control System

The delay control system consists essentially of a reversible binary counter which acts as a register of delay in the switched delay unit and provides signals to control it. Fig. 5 shows a block diagram of the delay system. The counter is supplied with line synchronising pulses (identical with one of the inputs to the timing comparator). When a synchronising pulse is applied, the counter may either increase its value by one unit, or decrease its value by one unit, or remain unchanged, according to the error signals $P$ and $Q$ from the timing comparator. The total duration of all the switched delays in circuit is arranged to correspond to the binary number in the counter; this is achieved by applying the counter waveforms to a code converter which generates signals that operate the switches. Thus, each time the counter increases or decreases its value by one unit, the switched delay likewise increases or decreases its duration by one delay unit.

The binary counter also supplies the information required to control the switched quartz delays. By appropriately gating the outputs from the counter, one

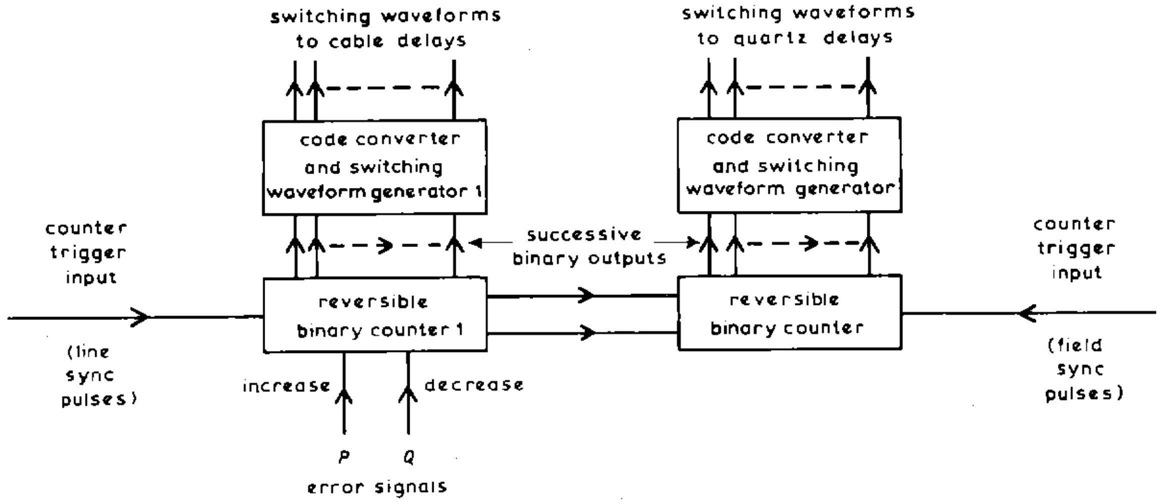
switching waveforms to cable delays
switching waveforms to quartz delays
code converter and switching waveform generator 1
code converter and switching waveform generator
counter trigger input
(line sync pulses)
successive binary outputs
reversible binary counter 1
reversible binary counter
counter trigger input
(field sync pulses)
increase
decrease
P
Q
error signals

*Fig. 5 - Delay control unit*

of two signals is derived indicating:

i) when the duration of the switched delays is greater than 240 units (i.e. near the maximum of 255).

or ii) when the duration of switched delays is less than 16 units (i.e. near the minimum of 0).

These two signals are used to control further stages of reversible binary counting. The count is triggered by field synchronising pulses and at the time of each pulse the value standing in the counter is changed so as to increase the delay in the quartz if the duration of the switched cable delay is greater than 240 units, or to reduce the quartz delay if it is less than 16 units. If neither of these conditions holds then the delay in the switched quartz section remains unchanged. If a change of quartz delay does occur it is necessary also to change the value of the switched cable delay so that the total delay remains approximately unaltered. This is achieved by switching the first reversible counter also to a value near the opposite end of its range. There still remains the error of a few units and this is corrected by the normal action of the switched cable delay during the field blanking interval.

## 4. PERFORMANCE OF SYSTEM

The rate of change of delay in the switched cable delay system is 9 ns per line, i.e. approximately 2½ μs per field or 140 μs per second. However, the quartz delays can only be changed once per field and, in the limit, this means that changes of greater than 16 x 9 ns i.e. 0·144 μs per field cannot be accommodated; in practice the rate of change of frequency is found to be very small and does not cause any difficulties. When first switching on, however, five fields may elapse before the servo-system is operating correctly.

## 5. CONCLUSIONS

A delay control system has been described which enables the duration of a field delay to be held equal to the field duration of an input television signal. The system has a range of plus or minus 4 μs which enables it to handle field frequency variations of approximately one part in five thousand.

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## APPENDIX

The logic diagram of one stage of the reversible counter is shown in Fig. 6.*

Counting is performed in a triggered J-K flip-flop which changes state when both J and K are 'O' but remain unchanged when both are '1'. Signals are transmitted to the next stage through controlling gate circuits.

A common trigger signal is applied to every stage to ensure synchronous action of the counters and two control signals determine whether counting upwards or downwards takes place. If both control signals are '1' no counting can take place since the J and K inputs are both '1'. If, however, one of these signals is 'O' (and the other is '1') a signal is transmitted from one stage to the next in the conventional manner, from Q for counting upwards and from $\overline{Q}$ (the inverse of Q) for counting downwards.

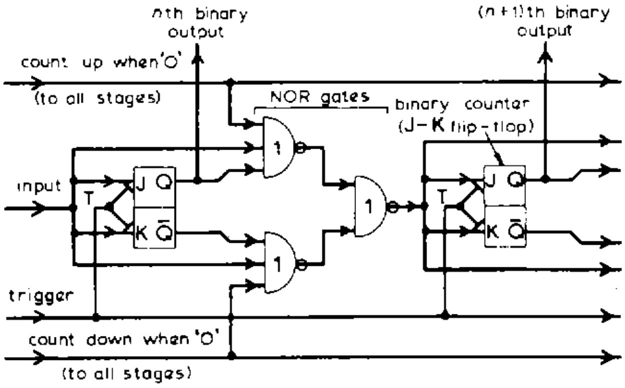

*Fig. 6 - One stage of reversible binary counter*

* The counter is an extension of a standard synchronous counter using integrated circuits. Reference to such counters can be found in the integrated circuit manufacturers design information. This counter was designed to use 'Motorola' integrated circuits.

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